

Figure 1a (related art)

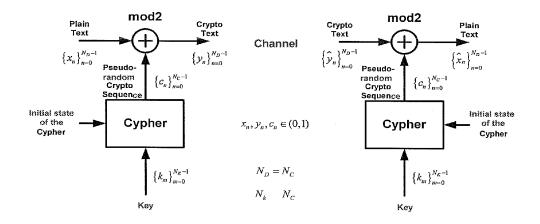


Figure 1b (related art)

Initial state of the Cypher

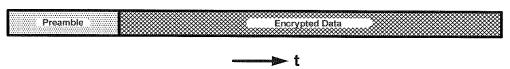


Figure 1c (related art)

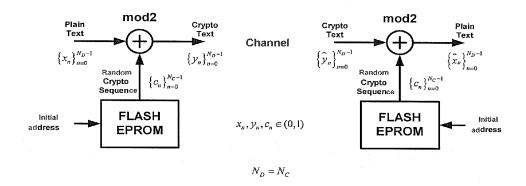


Figure 2a

Initial address

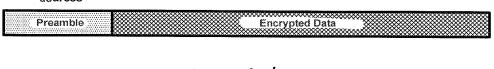


Figure 2b

FLASH EPROM

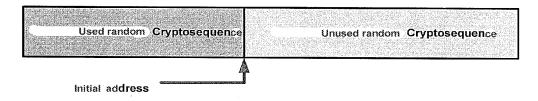


Figure 2c

FLASH EPROM

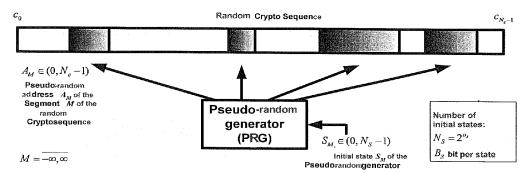


Figure 3a

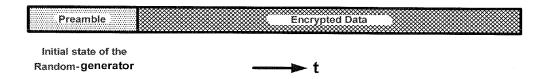


Figure 3b

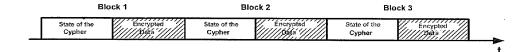


Figure 4a (related art)

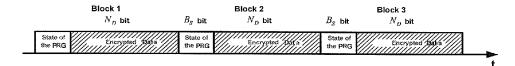


Figure 4b

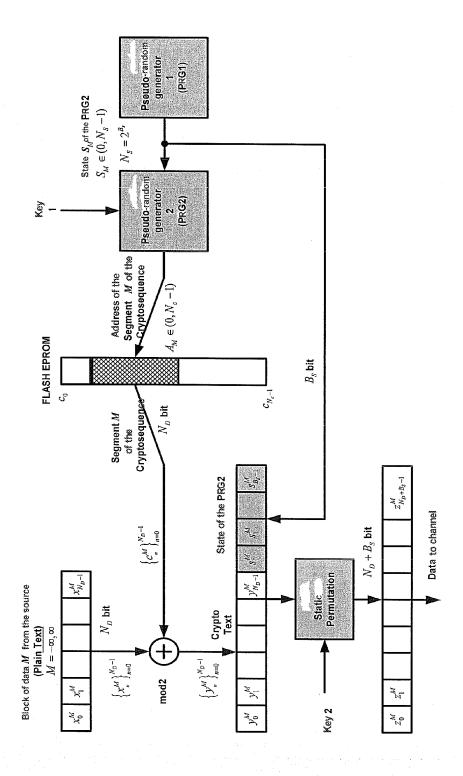


Figure 5

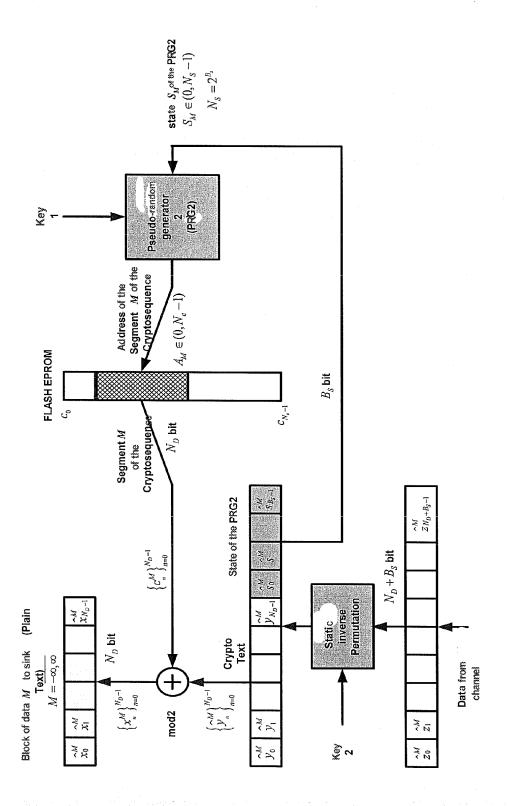


Figure 6